# 200 MHz Clock Generator PLL

# ADF4001

## FEATURES

**200 MHz Bandwidth**
**2.7 V to 5.5 V Power Supply**
**Separate Charge Pump Supply ($V_P$) Allows Extended Tuning Voltage in 5 V Systems**
**Programmable Charge Pump Currents**
**3-Wire Serial Interface**
**Hardware and Software Power-Down Mode**
**Analog and Digital Lock Detect**
**Hardware Compatible to the ADF4110/ADF4111/ ADF4112/ADF4113**
**Typical Operating Current 4.5 mA**
**Ultralow Phase Noise**
**16-Lead TSSOP**
**20-Lead LFCSP**

## APPLICATIONS

**Clock Generation**
**Low Frequency PLLs**
**Low Jitter Clock Source**
**Clock Smoothing**
**Frequency Translation**
**SONET, ATM, ADM, DSLAM, SDM**

## GENERAL DESCRIPTION

The ADF4001 clock generator can be used to implement clock sources for PLLs that require very low noise, stable reference signals. It consists of a low noise digital PFD (phase frequency detector), a precision charge pump, a programmable reference divider, and a programmable 13-bit N counter. In addition, the 14-bit reference counter (R counter) allows selectable $REF_{IN}$ frequencies at the PFD input. A complete PLL (phase-locked loop) can be implemented if the synthesizer is used with an external loop filter and VCO (voltage controlled oscillator) or VCXO (voltage controlled crystal oscillator). The N minimum value of 1 allows flexibility in clock generation.

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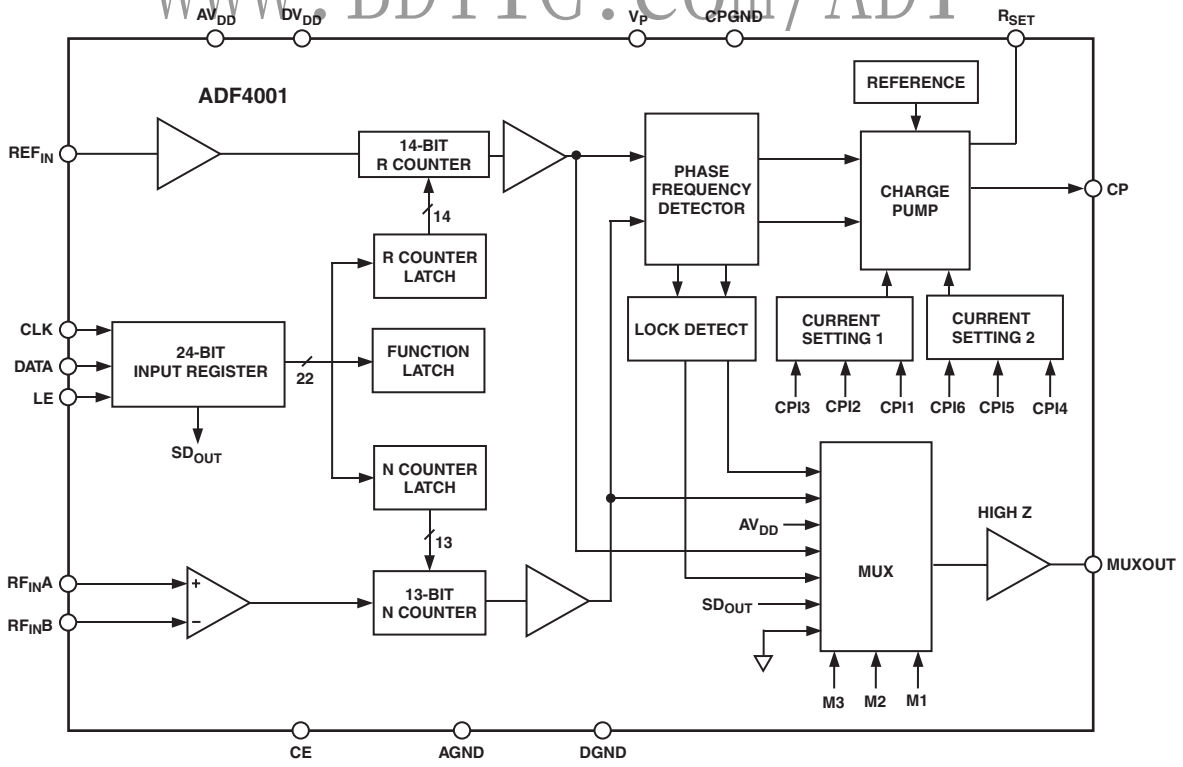
## FUNCTIONAL BLOCK DIAGRAM




REV. A

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# ADF4001–SPECIFICATIONS[1]

**($AV_{DD}$ = $DV_{DD}$ = 3 V ± 10%, 5 V ± 10%; $AV_{DD} \le V_P \le 6.0$ V; AGND = DGND = CPGND = 0 V; $R_{SET}$ = 4.7 kΩ; $T_A = T_{MIN}$ to $T_{MAX}$, unless otherwise noted; dBm referred to 50 Ω.)**

| Parameter | B Version | Unit | Test Conditions/Comments |
|---|---|---|---|
| RF CHARACTERISTICS (3 V) | | | See Figure 3 for Input Circuit |
| RF Input Frequency | 5/165 | MHz min/max | |
| RF Input Sensitivity | –10/0 | dBm min/max | |
| RF CHARACTERISTICS (5 V) | | | |
| RF Input Frequency | 10/200 | MHz min/max | –5/0 dBm min/max |
| | 20/200 | MHz min/max | –10/0 dBm min/max |
| $REF_{IN}$ CHARACTERISTICS | | | See Figure 2 for Input Circuit |
| $REF_{IN}$ Input Frequency | 5/104 | MHz min/max | For f < 5 MHz, Use DC-Coupled Square Wave (0 to $V_{DD}$) |
| $REF_{IN}$ Input Sensitivity[2] | –5 | dBm min | AC-Coupled. When DC-Coupled: 0 to $V_{DD}$ Max (CMOS Compatible) |
| $REF_{IN}$ Input Capacitance | 10 | pF max | |
| $REF_{IN}$ Input Current | ±100 | µA max | |
| PHASE DETECTOR | | | |
| Phase Detector Frequency[3] | 55 | MHz max | |
| CHARGE PUMP | | | |
| $I_{CP}$ Sink/Source | | | Programmable: See Table V |
| High Value | 5 | mA typ | With $R_{SET}$ = 4.7 kΩ |
| Low Value | 625 | µA typ | |
| Absolute Accuracy | 2.5 | % typ | With $R_{SET}$ = 4.7 kΩ |
| $R_{SET}$ Range | 2.7/10 | kΩ typ | See Table V |
| $I_{CP}$ Three-State Leakage Current | 1 | nA typ | |
| Sink and Source Current Matching | 2 | % typ | 0.5 V ≤ $V_{CP}$ ≤ $V_P$ – 0.5 |
| $I_{CP}$ vs. $V_{CP}$ | 1.5 | % typ | 0.5 V ≤ $V_{CP}$ ≤ $V_P$ – 0.5 |
| $I_{CP}$ vs. Temperature | 2 | % typ | $V_{CP}$ = $V_P$/2 |
| LOGIC INPUTS | | | |
| $V_{INH}$, Input High Voltage | 0.8 × $DV_{DD}$ | V min | |
| $V_{INL}$, Input Low Voltage | 0.2 × $DV_{DD}$ | V max | |
| $I_{INH}/I_{INL}$, Input Current | ±1 | µA max | |
| $C_{IN}$, Input Capacitance | 10 | pF max | |
| LOGIC OUTPUTS | | | |
| $V_{OH}$, Output High Voltage | $DV_{DD}$ – 0.4 | V min | $I_{OH}$ = 500 µA |
| $V_{OL}$, Output Low Voltage | 0.4 | V max | $I_{OL}$ = 500 µA |
| POWER SUPPLIES | | | |
| $AV_{DD}$ | 2.7/5.5 | V min/V max | |
| $DV_{DD}$ | $AV_{DD}$ | | |
| $V_P$ | $AV_{DD}$/6.0 | V min/V max | $AV_{DD} \le V_P \le 6.0$ V |
| $I_{DD}$[4] ($AI_{DD}$ + $DI_{DD}$) | | | |
| ADF4001 | 5.5 | mA max | 4.5 mA typical |
| $I_P$ | 0.4 | mA max | $T_A$ = 25°C |
| Low Power Sleep Mode | 1 | µA typ | |
| NOISE CHARACTERISTICS | | | |
| ADF4001 Phase Noise Floor[5] | –161 | dBc/Hz typ | @ 200 kHz PFD Frequency |
| | –153 | dBc/Hz typ | @ 1 MHz PFD Frequency |
| Phase Noise Performance[6] | | | @ VCXO Output |
| 200 MHz Output[7] | –99 | dBc/Hz typ | @ 1 kHz Offset and 200 kHz PFD Frequency |
| Spurious Signals | | | |
| 200 MHz Output[7] | –90/–95 | dBc typ/dBc typ | @ 200 kHz/400 kHz and 200 kHz PFD Frequency |

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NOTES

[1]Operating temperature range (B Version) is –40°C to +85°C.

[2]$AV_{DD}$ = $DV_{DD}$ = 3 V; for $AV_{DD}$ = $DV_{DD}$ = 5 V, use CMOS compatible levels.

[3]Guaranteed by design. Sample tested to ensure compliance.

[4]$T_A$ = 25°C; $AV_{DD}$ = $DV_{DD}$ = 3 V; $RF_{IN}$ = 100 MHz.

[5]The synthesizer phase noise floor is estimated by measuring the in-band phase noise at the output of the VCO and subtracting 20 logN (where N is the N divider value).

[6]The phase noise is measured with the EVAL-ADF4001EB1 evaluation board and the HP8562E spectrum analyzer.

[7]$f_{REF_{IN}}$ = 10 MHz; $f_{PFD}$ = 200 kHz; Offset Frequency = 1 kHz; $f_{RF}$ = 200 MHz; N = 1000; Loop B/W = 20 kHz.

Specifications subject to change without notice.

## TIMING CHARACTERISTICS ($AV_{DD}$ = $DV_{DD}$ = 3 V ± 10%, 5 V ± 10%; $AV_{DD} \le V_P \le 6.0$ V; AGND = DGND = CPGND= 0 V; $R_{SET}$ = 4.7 kΩ; $T_A$ = $T_{MIN}$ to $T_{MAX}$, unless otherwise noted; dBm referred to 50 Ω.)

| Parameter | Limit at $T_{MIN}$ to $T_{MAX}$ (B Version) | Unit | Test Conditions/Comments |
|---|---|---|---|
| $t_1$ | 10 | ns min | DATA to CLOCK Setup Time |
| $t_2$ | 10 | ns min | DATA to CLOCK Hold Time |
| $t_3$ | 25 | ns min | CLOCK High Duration |
| $t_4$ | 25 | ns min | CLOCK Low Duration |
| $t_5$ | 10 | ns min | CLOCK to LE Setup Time |
| $t_6$ | 20 | ns min | LE Pulsewidth |

Guaranteed by design but not production tested.
Specifications subject to change without notice.

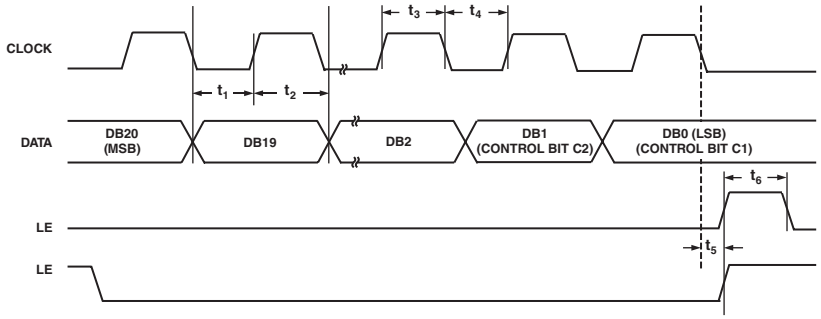


*Figure 1. Timing Diagram*

**ABSOLUTE MAXIMUM RATINGS**[1, 2]
($T_A$ = 25°C, unless otherwise noted.)

$AV_{DD}$ to GND[3] ..... –0.3 V to +7 V
$AV_{DD}$ to $DV_{DD}$ ..... 0 V to +0.3 V
$V_P$ to GND ..... –0.3 V to +7 V
$V_P$ to $AV_{DD}$ ..... –0.3 V to +5.5 V
Digital I/O Voltage to GND ..... –0.3 V to $V_{DD}$ + 0.3 V
Analog I/O Voltage to GND ..... –0.3 V to $V_P$ + 0.3 V
$REF_{IN}$, $RF_{IN}A$, $RF_{IN}B$ to GND ..... –0.3 V to $V_{DD}$ + 0.3 V
$RF_{IN}A$ to $RF_{IN}B$ ..... ±320 mV
Operating Temperature Range
Industrial (B Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Maximum Junction Temperature .....150°C
TSSOP $\theta_{JA}$ Thermal Impedance ..... 150.4°C/W
LFCSP $\theta_{JA}$ Thermal Impedance (Paddle Soldered) .. 122°C/W
LFCSP $\theta_{JA}$ Thermal Impedance (Paddle Not Soldered) 216°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... 215°C
Infrared (15 sec) ..... 220°C

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NOTES
[1]Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[2]This device is a high performance RF integrated circuit with an ESD rating of <2 kΩ and it is ESD sensitive. Proper precautions should be taken for handling and assembly.
[3]GND = AGND = DGND = 0 V.

**ORDERING GUIDE**

| Model | Temperature Range | Package Description | Package Option |
|---|---|---|---|
| ADF4001BRU | –40°C to +85°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADF4001BRU-REEL | –40°C to +85°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADF4001BRU-REEL7 | –40°C to +85°C | Thin Shrink Small Outline Package (TSSOP) | RU-16 |
| ADF4001BCP | –40°C to +85°C | Lead Frame Chip Scale Package (LFCSP)* | CP-20 |
| ADF4001BCP-REEL | –40°C to +85°C | Lead Frame Chip Scale Package (LFCSP)* | CP-20 |
| ADF4001BCP-REEL7 | –40°C to +85°C | Lead Frame Chip Scale Package (LFCSP)* | CP-20 |
| EVAL-ADF4001EB2 | | Evaluation Board | |

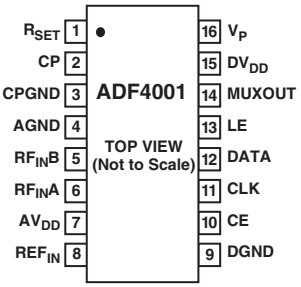
*Contact factory for chip availability.

**CAUTION**

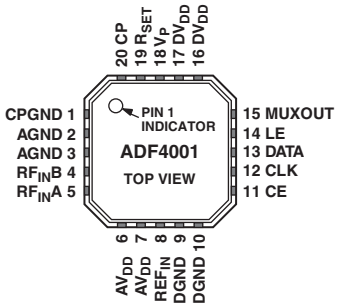
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADF4001 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

## PIN CONFIGURATIONS

**TSSOP**




**LFCSP**




NOTE: TRANSISTOR COUNT 6425 (CMOS) AND 50 (BIPOLAR)

## PIN FUNCTION DESCRIPTIONS

| TSSOP Pin No. | LFCSP Pin No. | Mnemonic | Function |
|---|---|---|---|
| 1 | 19 | $R_{SET}$ | Connecting a resistor between this pin and CPGND sets the maximum charge pump output current. The nominal voltage potential at the $R_{SET}$ pin is 0.66 V. The relationship between $I_{CP}$ and $R_{SET}$ is $$I_{CP\ MAX} = \frac{23.5}{R_{SET}}$$ So, with $R_{SET}$ = 4.7 kΩ, $I_{CP\ MAX}$ = 5 mA. |
| 2 | 20 | CP | Charge Pump Output. When enabled, this provides $\pm I_{CP}$ to the external loop filter which, in turn, drives the external VCO or VCXO. |
| 3 | 1 | CPGND | Charge Pump Ground. This is the ground return path for the charge pump. |
| 4 | 2, 3 | AGND | Analog Ground. This is the ground return path of the prescaler. |
| 5 | 4 | $RF_{IN}B$ | Complementary Input to the N counter. This point must be decoupled to the ground plane with a small bypass capacitor, typically 100 pF. See Figure 3. |
| 6 | 5 | $RF_{IN}A$ | Input to the N counter. This small signal input is ac-coupled to the external VCO or VCXO. |
| 7 | 6, 7 | $AV_{DD}$ | Analog Power Supply. This ranges from 2.7 V to 5.5 V. Decoupling capacitors to the analog ground plane should be placed as close as possible to this pin. $AV_{DD}$ must have the same value as $DV_{DD}$. |
| 8 | 8 | $REF_{IN}$ | Reference Input. This is a CMOS input with a nominal threshold of $V_{DD}/2$ and a dc equivalent input resistance of 100 kΩ. See Figure 2. This input can be driven from a TTL or CMOS crystal oscillator or can be ac-coupled. |
| 9 | 9, 10 | DGND | Digital Ground. |
| 10 | 11 | CE | Chip Enable. A logic low on this pin powers down the device and puts the charge pump output into three-state mode. Taking the pin high will power up the device, depending on the status of the power-down bit F2. |
| 11 | 12 | CLK | Serial Clock Input. This serial clock is used to clock in the serial data to the registers. The data is latched into the 24-bit shift register on the CLK rising edge. This input is a high impedance CMOS input. |
| 12 | 13 | DATA | Serial Data Input. The serial data is loaded MSB first with the two LSBs being the control bits. This input is a high impedance CMOS input. |
| 13 | 14 | LE | Load Enable, CMOS Input. When LE goes high, the data stored in the shift registers is loaded into one of the four latches, the latch being selected by using the control bits. |
| 14 | 15 | MUXOUT | This multiplexer output allows either the lock detect, the scaled RF, or the scaled reference frequency to be accessed externally. |
| 15 | 16, 17 | $DV_{DD}$ | Digital Power Supply. This ranges from 2.7 V to 5.5 V. Decoupling capacitors to the digital ground plane should be placed as close as possible to this pin. $DV_{DD}$ must be the same value as $AV_{DD}$. |
| 16 | 18 | $V_P$ | Charge Pump Power Supply. This should be greater than or equal to $V_{DD}$. In systems where $V_{DD}$ is 3 V, it can be set to 5 V and used to drive a VCO or VCXO with a tuning range of up to 5 V. |

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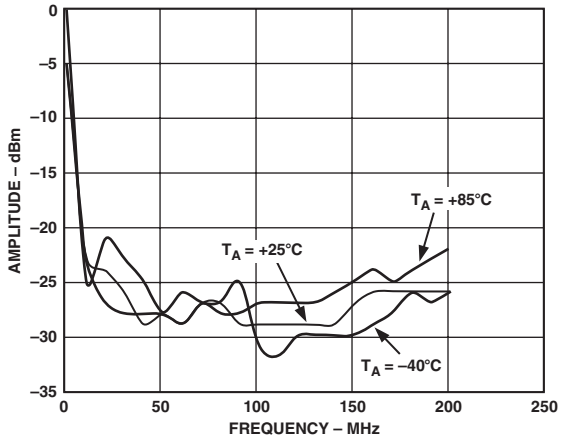
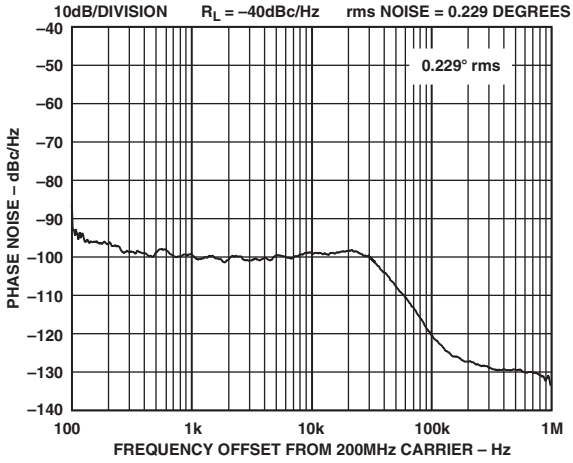
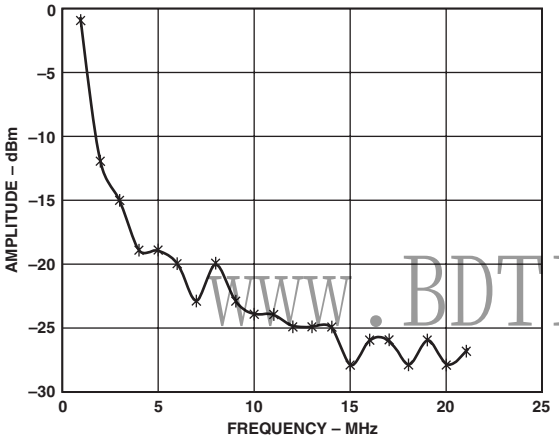


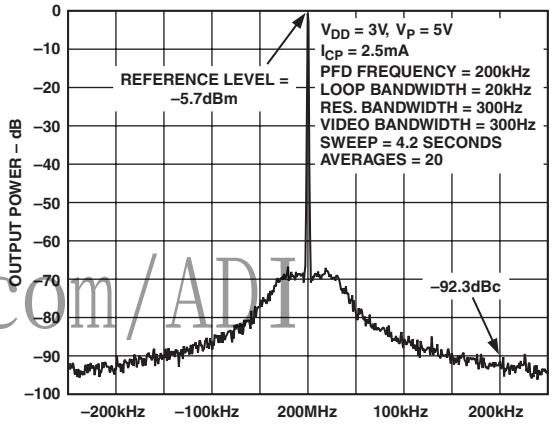

TPC 1. Input Sensitivity, $V_{DD}$ = 3.3 V, 100 pF on $RF_{IN}$




TPC 4. Integrated Phase Noise (200 MHz, 200 kHz, 20 kHz)




TPC 2. Input Sensitivity, $V_{DD}$ = 3.3 V, 100 pF on $RF_{IN}$




TPC 5. Reference Spurs (200 MHz, 200 kHz, 20 kHz)

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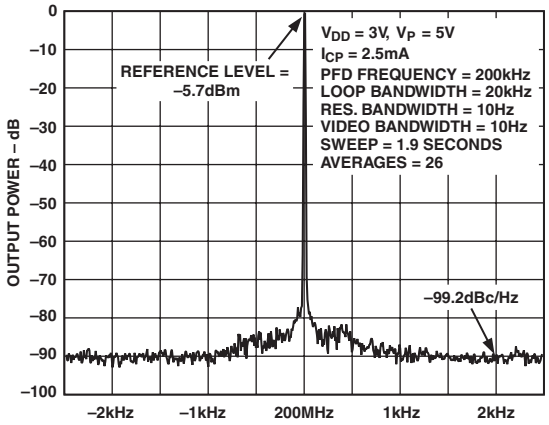


TPC 3. Phase Noise (200 MHz, 200 kHz, 20 kHz)

## CIRCUIT DESCRIPTION

### Reference Input Section

The reference input stage is shown in Figure 2. SW1 and SW2 are normally closed switches. SW3 is normally open. When power-down is initiated, SW3 is closed and SW1 and SW2 are opened. This ensures that there is no loading of the $REF_{IN}$ pin on power-down.

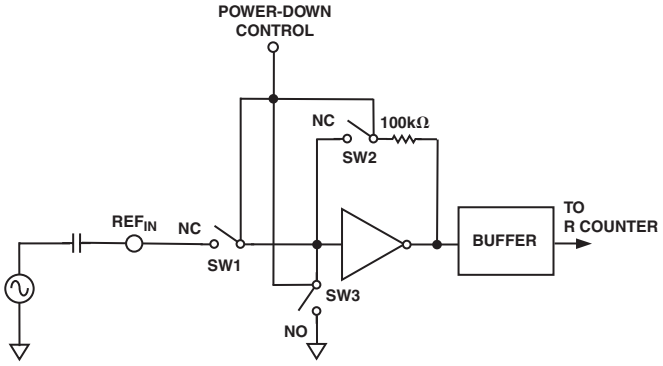


*Figure 2. Reference Input Stage*

### RF Input Stage

The RF input stage is shown in Figure 3. It is followed by a two-stage limiting amplifier to generate the CML clock levels needed for the N counter buffer.

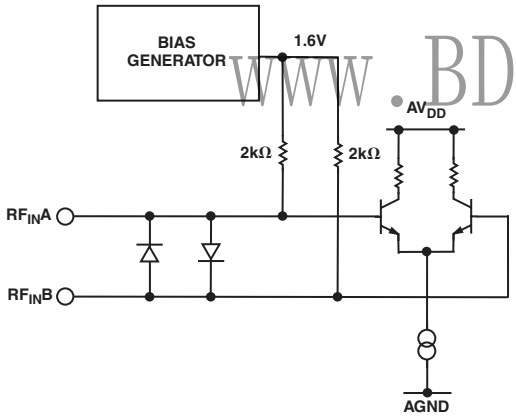


*Figure 3. RF Input Stage*

### N Counter

The N CMOS counter allows a wide ranging division ratio in the PLL feedback counter. Division ratios of 1 to 8191 are allowed.

***N and R Relationship***

The N counter with the R counter make it possible to generate output frequencies that are spaced only by the reference frequency divided by *R*. The equation for the VCO frequency is

$$f_{VCO} = N/R \times f_{REFIN}$$

$f_{VCO}$ is the output frequency of the external voltage cotrolled oscillator (VCO).

*N* is the preset divide ratio of the binary 13-bit counter (1 to 8,191).

$f_{REFIN}$ is the external reference frequency oscillator.

*R* is the preset divide ratio of the binary 14-bit programmable reference counter (1 to 16,383).

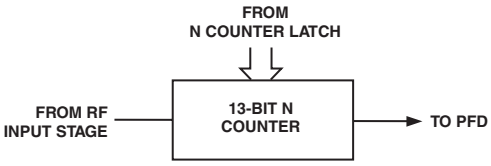


*Figure 4. N Counter*

### R Counter

The 14-bit R counter allows the input reference frequency to be divided down to produce the reference clock to the phase frequency detector (PFD). Division ratios from 1 to 16,383 are allowed.

## PHASE FREQUENCY DETECTOR (PFD) AND CHARGE PUMP

The PFD takes inputs from the R counter and N counter and produces an output proportional to the phase and frequency difference between them. Figure 5 is a simplified schematic. The PFD includes a programmable delay element that controls the width of the antibacklash pulse. This pulse ensures that no dead zone is in the PFD transfer function and minimizes phase noise and reference spurs. Two bits in the reference counter latch, ABP2 and ABP1, control the width of the pulse (see Table III).

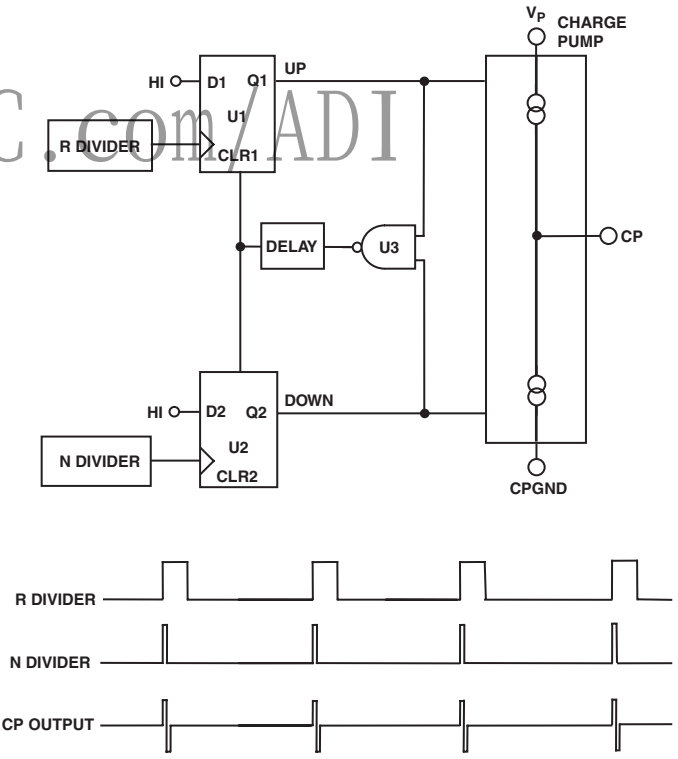


*Figure 5. PFD Simplified Schematic and Timing (In Lock)*

## MUXOUT AND LOCK DETECT

The output multiplexer on the ADF4001 family allows the user to access various internal points on the chip. The state of MUXOUT is controlled by M3, M2, and M1 in the function latch. Table V shows the full truth table. Figure 6 shows the MUXOUT section in block diagram form.

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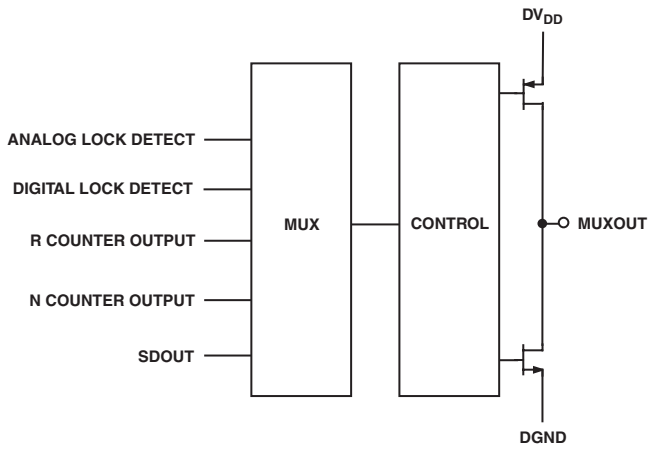


*Figure 6. MUXOUT Circuit*

**Lock Detect**

MUXOUT can be programmed for two types of lock detect: digital lock detect and analog lock detect. Digital lock detect is active high. When LDP in the R counter latch is set to 0, digital lock detect is set high when the phase error on three consecutive phase detector cycles is less than 15 ns. With LDP set to 1, five consecutive cycles of less than 15 ns are required to set the lock detect. It will stay set high until a phase error of greater than 25 ns is detected on any subsequent PD cycle. The N-channel open-drain analog lock detect should be operated with an external pull-up resistor of 10 kΩ nominal. When lock has been detected, this output will be high with narrow low-going pulses.

**INPUT SHIFT REGISTER**

The ADF4001 digital section includes a 24-bit input shift register, a 14-bit R counter, and a 13-bit N counter. Data is clocked into the 24-bit shift register on each rising edge of CLK. The data is clocked in MSB first. Data is transferred from the shift register to one of four latches on the rising edge of LE. The destination latch is determined by the state of the two control bits (C2, C1) in the shift register. These are the two LSBs, DB1 and DB0, as shown in the timing diagram of Figure 1. The truth table for these bits is shown in Table I. Table II shows a summary of how the latches are programmed.

**Table I. C2, C1 Truth Table**

| Control Bits | | |
|---|---|---|
| C2 | C1 | Data Latch |
| 0 | 0 | R Counter |
| 0 | 1 | N Counter |
| 1 | 0 | Function Latch |
| 1 | 1 | Initialization Latch |

**Table II. ADF4001 Family Latch Summary**

**REFERENCE COUNTER LATCH**

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| RESERVED | | | LOCK DETECT PRECISION | TEST MODE BITS | | ANTI-BACKLASH WIDTH | | 14-BIT REFERENCE COUNTER | | | | | | | | | | | | | CONTROL BITS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| X | X | X | LDP | T2 | T1 | ABP2 | ABP1 | R14 | R13 | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | C2 (0) | C1 (0) |

**N COUNTER LATCH**

| RESERVED | | CP GAIN | 13-BIT N COUNTER | | | | | | | | | | | | | RESERVED | | | | | | CONTROL BITS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| X | X | G1 | N13 | N12 | N11 | N10 | N9 | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | X | X | X | X | X | X | C2 (0) | C1 (1) |

**FUNCTION LATCH**

| RESERVED | | POWER-DOWN 2 | CURRENT SETTING 2 | | | CURRENT SETTING 1 | | | TIMER COUNTER CONTROL | | | | FASTLOCK MODE | FASTLOCK ENABLE | CP THREE-STATE | PHASE DETECTOR POLARITY | MUXOUT CONTROL | | | POWER-DOWN 1 | COUNTER RESET | CONTROL BITS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| X | X | PD2 | CPI6 | CPI5 | CPI4 | CPI3 | CPI2 | CPI1 | TC4 | TC3 | TC2 | TC1 | F5 | F4 | F3 | F2 | M3 | M2 | M1 | PD1 | F1 | C2 (1) | C1 (0) |

**INITIALIZATION LATCH**

| RESERVED | | POWER-DOWN 2 | CURRENT SETTING 2 | | | CURRENT SETTING 1 | | | TIMER COUNTER CONTROL | | | | FASTLOCK MODE | FASTLOCK ENABLE | CP THREE-STATE | PHASE DETECTOR POLARITY | MUXOUT CONTROL | | | POWER-DOWN 1 | COUNTER RESET | CONTROL BITS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| X | X | PD2 | CPI6 | CPI5 | CPI4 | CPI3 | CPI2 | CPI1 | TC4 | TC3 | TC2 | TC1 | F5 | F4 | F3 | F2 | M3 | M2 | M1 | PD1 | F1 | C2 (1) | C1 (1) |

X = DON'T CARE

**Table III. Reference Counter Latch Map**

| RESERVED | | | LOCK DETECT PRECISION | TEST MODE BITS | | ANTI-BACKLASH WIDTH | | 14-BIT REFERENCE COUNTER | | | | | | | | | | | | | | CONTROL BITS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| X | X | X | LDP | T2 | T1 | ABP2 | ABP1 | R14 | R13 | R12 | R11 | R10 | R9 | R8 | R7 | R6 | R5 | R4 | R3 | R2 | R1 | C2 (0) | C1 (0) |

X = DON'T CARE

| R14 | R13 | R12 | ..... | R3 | R2 | R1 | DIVIDE RATIO |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | ..... | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | ..... | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | ..... | 0 | 1 | 1 | 3 |
| 0 | 0 | 0 | ..... | 1 | 0 | 0 | 4 |
| . | . | . | ..... | . | . | . | . |
| . | . | . | ..... | . | . | . | . |
| . | . | . | ..... | . | . | . | . |
| 1 | 1 | 1 | ..... | 1 | 0 | 0 | 16380 |
| 1 | 1 | 1 | ..... | 1 | 0 | 1 | 16381 |
| 1 | 1 | 1 | ..... | 1 | 1 | 0 | 16382 |
| 1 | 1 | 1 | ..... | 1 | 1 | 1 | 16383 |

| ABP2 | ABP1 | ANTIBACKLASH PULSE WIDTH |
|---|---|---|
| 0 | 0 | 2.9ns |
| 0 | 1 | 1.3ns |
| 1 | 0 | 6.0ns |
| 1 | 1 | 2.9ns |

TEST MODE BITS SHOULD BE SET TO 00 FOR NORMAL OPERATION

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| LDP | OPERATION |
|---|---|
| 0 | THREE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET. |
| 1 | FIVE CONSECUTIVE CYCLES OF PHASE DELAY LESS THAN 15ns MUST OCCUR BEFORE LOCK DETECT IS SET. |

**Table IV. N Counter Latch Map**

| RESERVED | | CP GAIN | 13-BIT N COUNTER | | | | | | | | | | | | | RESERVED | | | | | | CONTROL BITS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| X | X | G1 | N13 | N12 | N11 | N10 | N9 | N8 | N7 | N6 | N5 | N4 | N3 | N2 | N1 | X | X | X | X | X | X | C2 (0) | C1 (1) |

X = DON'T CARE

| N13 | N12 | N11 | ..... | N3 | N2 | N1 | N COUNTER DIVIDE RATIO |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | ..... | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | ..... | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | ..... | 0 | 1 | 1 | 3 |
| 0 | 0 | 0 | ..... | 1 | 0 | 0 | 4 |
| . | . | . | ..... | . | . | . | . |
| . | . | . | ..... | . | . | . | . |
| . | . | . | ..... | . | . | . | . |
| 1 | 1 | 1 | ..... | 1 | 0 | 0 | 8188 |
| 1 | 1 | 1 | ..... | 1 | 0 | 1 | 8189 |
| 1 | 1 | 1 | ..... | 1 | 1 | 0 | 8190 |
| 1 | 1 | 1 | ..... | 1 | 1 | 1 | 8191 |

| F4 (FUNCTION LATCH) FASTLOCK ENABLE | CP GAIN | OPERATION |
|---|---|---|
| 0 | 0 | CHARGE PUMP CURRENT SETTING 1 IS PERMANENTLY USED |
| 0 | 1 | CHARGE PUMP CURRENT SETTING 2 IS PERMANENTLY USED |
| 1 | 0 | CHARGE PUMP CURRENT SETTING 1 IS USED |
| 1 | 1 | CHARGE PUMP CURRENT IS SWITCHED TO SETTING 2. THE TIME SPENT IN SETTING 2 IS DEPENDENT ON WHICH FASTLOCK MODE IS USED. SEE FUNCTION LATCH DESCRIPTION. |

THESE BITS ARE NOT USED BY THE DEVICE AND ARE DON'T CARE BITS.

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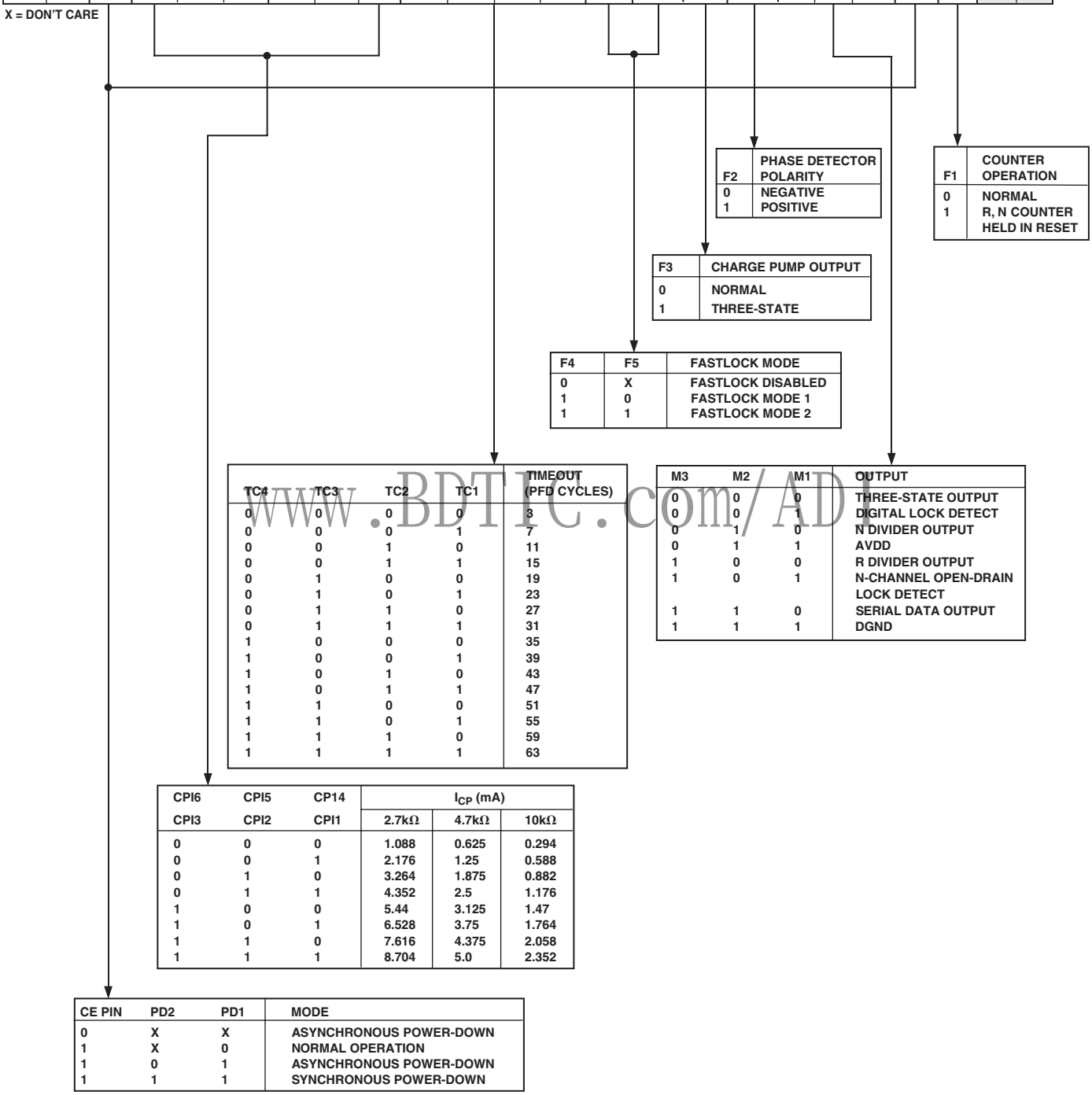
**Table V. Function Latch Map**

| RESERVED | | POWER-DOWN 2 | CURRENT SETTING 2 | | | CURRENT SETTING 1 | | | TIMER COUNTER CONTROL | | | | FASTLOCK MODE | FASTLOCK ENABLE | CP THREE-STATE | PHASE DETECTOR POLARITY | MUXOUT CONTROL | | | POWER-DOWN 1 | COUNTER RESET | CONTROL BITS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| X | X | PD2 | CPI6 | CPI5 | CPI4 | CPI3 | CPI2 | CPI1 | TC4 | TC3 | TC2 | TC1 | F5 | F4 | F3 | F2 | M3 | M2 | M1 | PD1 | F1 | C2 (1) | C1 (0) |

X = DON'T CARE



| F2 | PHASE DETECTOR POLARITY |
|---|---|
| 0 | NEGATIVE |
| 1 | POSITIVE |

| F1 | COUNTER OPERATION |
|---|---|
| 0 | NORMAL |
| 1 | R, N COUNTER HELD IN RESET |

| F3 | CHARGE PUMP OUTPUT |
|---|---|
| 0 | NORMAL |
| 1 | THREE-STATE |

| F4 | F5 | FASTLOCK MODE |
|---|---|---|
| 0 | X | FASTLOCK DISABLED |
| 1 | 0 | FASTLOCK MODE 1 |
| 1 | 1 | FASTLOCK MODE 2 |

| TC4 | TC3 | TC2 | TC1 | TIMEOUT (PFD CYCLES) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 3 |
| 0 | 0 | 0 | 1 | 7 |
| 0 | 0 | 1 | 0 | 11 |
| 0 | 0 | 1 | 1 | 15 |
| 0 | 1 | 0 | 0 | 19 |
| 0 | 1 | 0 | 1 | 23 |
| 0 | 1 | 1 | 0 | 27 |
| 0 | 1 | 1 | 1 | 31 |
| 1 | 0 | 0 | 0 | 35 |
| 1 | 0 | 0 | 1 | 39 |
| 1 | 0 | 1 | 0 | 43 |
| 1 | 0 | 1 | 1 | 47 |
| 1 | 1 | 0 | 0 | 51 |
| 1 | 1 | 0 | 1 | 55 |
| 1 | 1 | 1 | 0 | 59 |
| 1 | 1 | 1 | 1 | 63 |

| M3 | M2 | M1 | OUTPUT |
|---|---|---|---|
| 0 | 0 | 0 | THREE-STATE OUTPUT |
| 0 | 0 | 1 | DIGITAL LOCK DETECT |
| 0 | 1 | 0 | N DIVIDER OUTPUT |
| 0 | 1 | 1 | AVDD |
| 1 | 0 | 0 | R DIVIDER OUTPUT |
| 1 | 0 | 1 | N-CHANNEL OPEN-DRAIN LOCK DETECT |
| 1 | 1 | 0 | SERIAL DATA OUTPUT |
| 1 | 1 | 1 | DGND |

| CPI6 | CPI5 | CP14 | $I_{CP}$ (mA) | | |
|---|---|---|---|---|---|
| CPI3 | CPI2 | CPI1 | 2.7kΩ | 4.7kΩ | 10kΩ |
| 0 | 0 | 0 | 1.088 | 0.625 | 0.294 |
| 0 | 0 | 1 | 2.176 | 1.25 | 0.588 |
| 0 | 1 | 0 | 3.264 | 1.875 | 0.882 |
| 0 | 1 | 1 | 4.352 | 2.5 | 1.176 |
| 1 | 0 | 0 | 5.44 | 3.125 | 1.47 |
| 1 | 0 | 1 | 6.528 | 3.75 | 1.764 |
| 1 | 1 | 0 | 7.616 | 4.375 | 2.058 |
| 1 | 1 | 1 | 8.704 | 5.0 | 2.352 |

| CE PIN | PD2 | PD1 | MODE |
|---|---|---|---|
| 0 | X | X | ASYNCHRONOUS POWER-DOWN |
| 1 | X | 0 | NORMAL OPERATION |
| 1 | 0 | 1 | ASYNCHRONOUS POWER-DOWN |
| 1 | 1 | 1 | SYNCHRONOUS POWER-DOWN |

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**Table VI. Initialization Latch Map**

| RESERVED | | POWER-DOWN 2 | CURRENT SETTING 2 | | | CURRENT SETTING 1 | | | TIMER COUNTER CONTROL | | | | FASTLOCK MODE | FASTLOCK ENABLE | CP THREE-STATE | PHASE DETECTOR POLARITY | MUXOUT CONTROL | | | POWER-DOWN 1 | COUNTER RESET | CONTROL BITS | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DB23 | DB22 | DB21 | DB20 | DB19 | DB18 | DB17 | DB16 | DB15 | DB14 | DB13 | DB12 | DB11 | DB10 | DB9 | DB8 | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 |
| X | X | PD2 | CPI6 | CPI5 | CPI4 | CPI3 | CPI2 | CPI1 | TC4 | TC3 | TC2 | TC1 | F5 | F4 | F3 | F2 | M3 | M2 | M1 | PD1 | F1 | C2 (1) | C1 (1) |

X = DON'T CARE

| F2 | PHASE DETECTOR POLARITY |
|---|---|
| 0 | NEGATIVE |
| 1 | POSITIVE |

| F1 | COUNTER OPERATION |
|---|---|
| 0 | NORMAL |
| 1 | R, N COUNTER HELD IN RESET |

| F3 | CHARGE PUMP OUTPUT |
|---|---|
| 0 | NORMAL |
| 1 | THREE-STATE |

| F4 | F5 | FASTLOCK MODE |
|---|---|---|
| 0 | X | FASTLOCK DISABLED |
| 1 | 0 | FASTLOCK MODE 1 |
| 1 | 1 | FASTLOCK MODE 2 |

| TC4 | TC3 | TC2 | TC1 | TIMEOUT (PFD CYCLES) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 3 |
| 0 | 0 | 0 | 1 | 7 |
| 0 | 0 | 1 | 0 | 11 |
| 0 | 0 | 1 | 1 | 15 |
| 0 | 1 | 0 | 0 | 19 |
| 0 | 1 | 0 | 1 | 23 |
| 0 | 1 | 1 | 0 | 27 |
| 0 | 1 | 1 | 1 | 31 |
| 1 | 0 | 0 | 0 | 35 |
| 1 | 0 | 0 | 1 | 39 |
| 1 | 0 | 1 | 0 | 43 |
| 1 | 0 | 1 | 1 | 47 |
| 1 | 1 | 0 | 0 | 51 |
| 1 | 1 | 0 | 1 | 55 |
| 1 | 1 | 1 | 0 | 59 |
| 1 | 1 | 1 | 1 | 63 |

| M3 | M2 | M1 | OUTPUT |
|---|---|---|---|
| 0 | 0 | 0 | THREE-STATE OUTPUT |
| 0 | 0 | 1 | DIGITAL LOCK DETECT |
| 0 | 1 | 0 | N DIVIDER OUTPUT |
| 0 | 1 | 1 | AVDD |
| 1 | 0 | 0 | R DIVIDER OUTPUT |
| 1 | 0 | 1 | N-CHANNEL OPEN-DRAIN LOCK DETECT |
| 1 | 1 | 0 | SERIAL DATA OUTPUT |
| 1 | 1 | 1 | DGND |

| CPI6 | CPI5 | CP14 | $I_{CP}$ (mA) | | |
|---|---|---|---|---|---|
| CPI3 | CPI2 | CPI1 | 2.7kΩ | 4.7kΩ | 10kΩ |
| 0 | 0 | 0 | 1.088 | 0.625 | 0.294 |
| 0 | 0 | 1 | 2.176 | 1.25 | 0.588 |
| 0 | 1 | 0 | 3.264 | 1.875 | 0.882 |
| 0 | 1 | 1 | 4.352 | 2.5 | 1.176 |
| 1 | 0 | 0 | 5.44 | 3.125 | 1.47 |
| 1 | 0 | 1 | 6.528 | 3.75 | 1.764 |
| 1 | 1 | 0 | 7.616 | 4.375 | 2.058 |
| 1 | 1 | 1 | 8.704 | 5.0 | 2.352 |

| CE PIN | PD2 | PD1 | MODE |
|---|---|---|---|
| 0 | X | X | ASYNCHRONOUS POWER-DOWN |
| 1 | X | 0 | NORMAL OPERATION |
| 1 | 0 | 1 | ASYNCHRONOUS POWER-DOWN |
| 1 | 1 | 1 | SYNCHRONOUS POWER-DOWN |

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**FUNCTION LATCH**
With C2, C1 set to 1, 0, the on-chip function latch will be programmed. Table V shows the input data format for programming the function latch.

**Counter Reset**
DB2 (F1) is the counter reset bit. When this is 1, the R counter and the A, B counters are reset. For normal operation, this bit should be 0. Upon powering up, the F1 bit needs to be disabled, and the N counter resumes counting in close alignment with the R counter. (The maximum error is one prescaler cycle.)

**Power-Down**
DB3 (PD1) and DB21 (PD2) on the ADF4001 family provide programmable power-down modes. They are enabled by the CE pin.

When the CE pin is low, the device is immediately disabled regardless of the states of PD2, PD1.

In the programmed asynchronous power-down, the device powers down immediately after latching a 1 into Bit PD1, with the condition that PD2 has been loaded with a 0.

In the programmed synchronous power-down, the device power-down is gated by the charge pump to prevent unwanted frequency jumps. Once the power-down is enabled by writing a 1 into Bit PD1 (on condition that a 1 has also been loaded to PD2), the device will go into power-down on the occurrence of the next charge pump event.

When a power-down is activated (either synchronous or asynchronous mode, including CE pin activated power-down), the following events occur:

- All active dc current paths are removed.
- The R, N, and timeout counters are forced to their load state conditions.
- The charge pump is forced into three-state mode.
- The digital clock detect circuitry is reset.
- The $RF_{IN}$ input is debiased.
- The reference input buffer circuitry is disabled.
- The input register remains active and capable of loading and latching data.

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**MUXOUT Control**
The on-chip multiplexer is controlled by M3, M2, M1 on the ADF4001. Table V shows the truth table.

**Fastlock Enable Bit**
DB9 of the function latch is the fastlock enable bit. Only when this is 1 is fastlock enabled.

**Fastlock Mode Bit**
DB10 of the function latch is the fastlock mode bit. When fastlock is enabled, this bit determines which fastlock mode is used. If the fastlock mode bit is 0, fastlock mode 1 is selected; if the fastlock mode bit is 1, fastlock mode 2 is selected.

***Fastlock Mode 1***
The charge pump current is switched to the contents of Current Setting 2.

The device enters fastlock by having a 1 written to the CP gain bit in the N counter latch. The device exits fastlock by having a 0 written to the CP gain bit in the AB counter latch.

***Fastlock Mode 2***
The charge pump current is switched to the contents of Current Setting 2.

The device enters fastlock by having a 1 written to the CP gain bit in the N counter latch. The device exits fastlock under the control of the timer counter. After the timeout period determined by the value in TC4–TC1, the CP gain bit in the N counter latch is automatically reset to 0 and the device reverts to normal mode instead of fastlock. See Table V for the timeout periods.

**Timer Counter Control**
The user has the option of programming two charge pump currents. The intent is that the Current Setting 1 is used when the RF output is stable and the system is in a static state. Current Setting 2 is meant to be used when the system is dynamic and in a state of change (i.e., when a new output frequency is programmed). The normal sequence of events is as follows.

The user initially decides what the preferred charge pump currents are going to be. For example, they may choose 2.5 mA as Current Setting 1 and 5 mA as Current Setting 2.

At the same time, they must also decide how long they want the secondary current to stay active before reverting to the primary current. This is controlled by the Timer Counter Control Bits DB14 to DB11 (TC4–TC1) in the function latch. The truth table is given in Table V.

Now, when the user wishes to program a new output frequency, they can simply program the N counter latch with new value for N. At the same time, they can set the CP gain bit to a 1, which sets the charge pump with the value in CPI6–CPI4 for a period of time determined by TC4–TC1. When this time is up, the charge pump current reverts to the value set by CPI3–CPI1. At the same time, the CP gain bit in the N counter latch is reset to 0 and is now ready for the next time that the user wishes to change the frequency.

Note that there is an enable feature on the timer counter. It is enabled when Fastlock Mode 2 is chosen by setting the fastlock mode bit (DB10) in the function latch to 1.

**Charge Pump Currents**
CPI3, CPI2, CPI1 program Current Setting 1 for the charge pump. CPI6, CPI5, CPI4 program Current Setting 2 for the charge pump. The truth table is given in Table V.

**PD Polarity**
This bit sets the PD polarity bit (see Table V).

**CP Three-State**
This bit sets the CP output pin. With the bit set high, the CP output is put into three-state. With the bit set low, the CP output is enabled.

### INITIALIZATION LATCH

When C2, C1 = 1, 1, the initialization latch is programmed. This is essentially the same as the function latch (programmed when C2, C1 = 1, 0).

However, when the initialization latch is programmed, there is an additional internal reset pulse applied to the R and N counters. This pulse ensures that the N counter is at a load point when the N counter data is latched, and the device will begin counting in close phase alignment.

If the latch is programmed for synchronous power-down (the CE pin is high; PD1 bit is high; and PD2 bit is low), the internal pulse also triggers this power-down. The oscillator input buffer is unaffected by the internal reset pulse, so close phase alignment is maintained when counting resumes.

When the first N counter data is latched after initialization, the internal reset pulse is again activated. However, successive N counter loads will not trigger the internal reset pulse.

### DEVICE PROGRAMMING AFTER INITIAL POWER-UP

After initially powering up the device, there are three ways to program the device.

#### Initialization Latch Method

Apply $V_{DD}$.

Program the initialization latch (11 in 2 LSB of input word). Make sure that F1 bit is programmed to 0.

Do an R load (00 in 2 LSBs).

Do an N load (01 in 2 LSBs).

When the initialization latch is loaded, the following occurs:

1. The function latch contents are loaded.
2. An internal pulse resets the R, N, and timeout counters to load state conditions and also three-states the charge pump. Note that the prescaler band gap reference and the oscillator input buffer are unaffected by the internal reset pulse, allowing close phase alignment when counting resumes.
3. Latching the first N counter data after the initialization word will activate the same internal reset pulse. Successive N loads will not trigger the internal reset pulse unless there is another initialization.

#### CE Pin Method

Apply $V_{DD}$.

Bring CE low to put the device into power-down. This is an asynchronous power-down in that it happens immediately.

Program the function latch (10).
Program the R counter latch (00).
Program the N counter latch (01).

Bring CE high to take the device out of power-down. The R and AB counters will now resume counting in close alignment.

Note that after CE goes high, a duration of 1 µs may be required for the prescaler band gap voltage and oscillator input buffer bias to reach steady state.

CE can be used to power the device up and down to check for channel activity. The input register does not need to be reprogrammed each time the device is disabled and enabled as long as it has been programmed at least once after $V_{DD}$ was initially applied.

#### Counter Reset Method

Apply $V_{DD}$.

Do a function latch load (10 in 2 LSBs). As part of this, load 1 to the F1 bit. This enables the counter reset.

Do an R counter load (00 in 2 LSBs).

Do an N counter load (01 in 2 LSBs).

Do a function latch load (10 in 2 LSBs). As part of this, load 0 to the F1 bit. This disables the counter reset.

This sequence provides the same close alignment as the initialization method. It offers direct control over the internal reset. Note that counter reset holds the counters at load point and three-states the charge pump but does not trigger synchronous power-down. The counter reset method requires an extra function latch load compared to the initialization latch method.

### APPLICATION

#### Extremely Stable, Low Jitter Reference Clock for GSM Base Station Transmitter

Figure 7 shows the ADF4001 being used with a VCXO to produce an extremely stable, low jitter reference clock for a GSM base station local oscillator (LO).

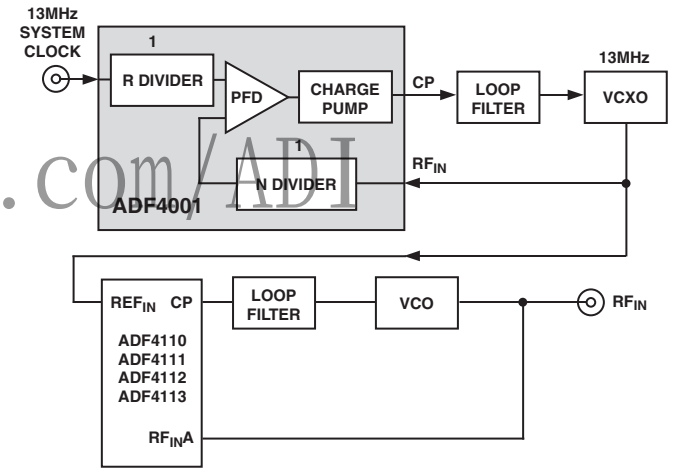


*Figure 7. Low Jitter, Stable Clock Source for GSM Base Station Local Oscillator Circuit*

The system reference signal is applied to the circuit at $REF_{IN}$. Typical GSM systems would have a very stable OCXO as the clock source for the entire base station. However, distribution of this signal around the base station makes it susceptible to noise and spurious pickup. It is also open to pulling from the various loads it may need to drive.

The charge pump output of the ADF4001 (Pin 2 of the TSSOP) drives the loop filter and the 13 MHz VCXO. The VCXO output is fed back to the RF input of the ADF4001 and also drives the reference ($REF_{IN}$) for the LO. A T-circuit configuration provides 50 Ω matching between the VCXO output, the LO $REF_{IN}$, and the $RF_{IN}$ terminal of the ADF4001.

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## COHERENT CLOCK GENERATION

When testing A/D converters, it is often advantageous to use a coherent test system, that is, a system that ensures a specific relationship between the A/D converter input signal and the A/D converter sample rate. Thus, when doing an FFT on this data, there is no longer any need to apply the window weighting function. Figure 8 shows how the ADF4001 can be used to handle all the possible combinations of the input signal frequency and sampling rate. The first ADF4001 is phase locked to a VCO. The output of the VCO is also fed into the N divider of the second ADF4001. This results in both ADF4001s being coherent with the $REF_{IN}$. Since the $REF_{IN}$ comes from the signal generator, the MUXOUT signal of the second ADF4001 is coherent with the $f_{IN}$ frequency to the ADC. This is used as $f_S$, the sampling clock.

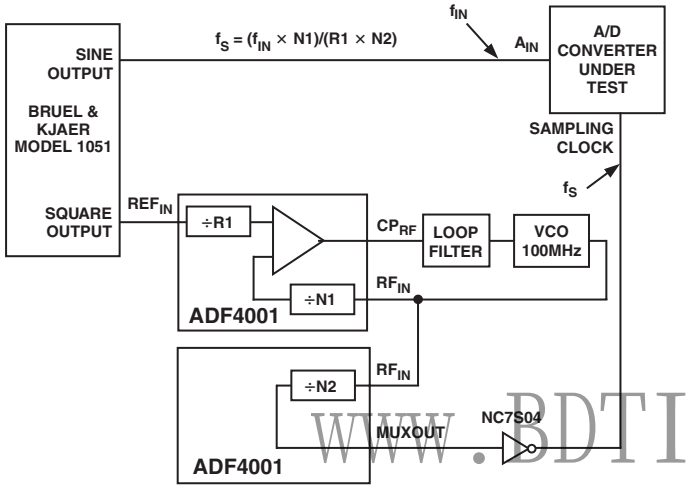


*Figure 8. Coherent Clock Generator*

## TRI-BAND CLOCK GENERATION CIRCUIT

In multiband applications, it is necessary to realize different clocks from one master clock frequency. For example, GSM uses a 13 MHz system clock, WCDMA uses 19.44 MHz, and CDMA uses 19.2 MHz. The circuit in Figure 9 shows how to use the ADF4001 to generate GSM, WCDMA, and CDMA system clocks from a single 52 MHz master clock. The low RF $f_{MIN}$ specification and the ability to program R and N values as low as ÷ 1 makes the ADF4001 suitable for this. Other $f_{OUT}$ clock frequencies can be realized using the formula

$$f_{OUT} = REF_{IN} \times (N \div R)$$

## SHUTDOWN CIRCUIT

The circuit in Figure 10 shows how to shut down both the ADF4001 and the accompanying VCO. The ADG702 switch goes open circuit when a Logic 1 is applied to the IN input. The low cost switch is available in both SOT-23 and micro SOIC packages.

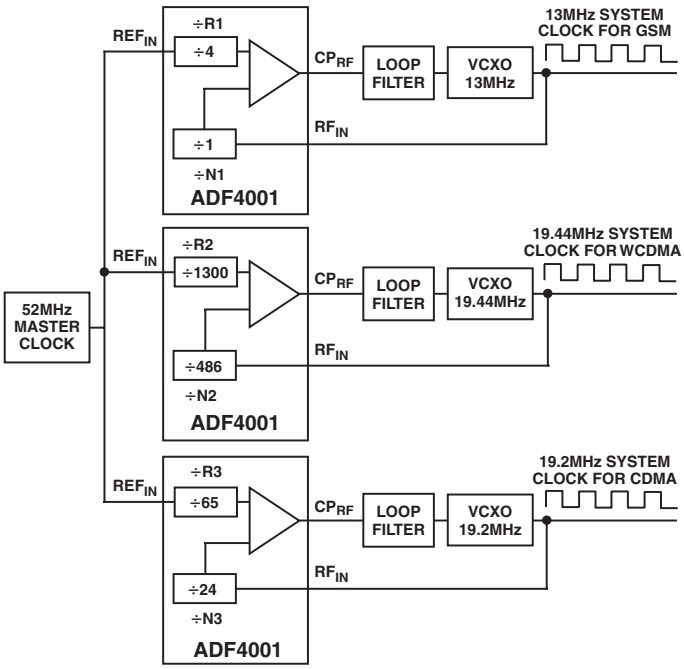


*Figure 9. Tri-Band System Clock Generation*

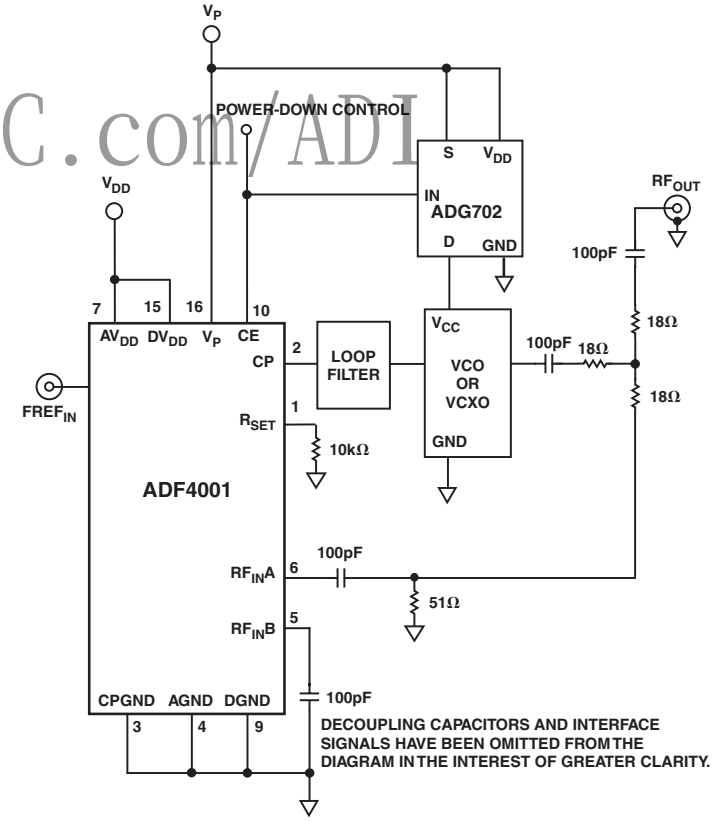


*Figure 10. Local Oscillator Shutdown Circuit*

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## INTERFACING

The ADF4001 family has a simple SPI® compatible serial interface for writing to the device. SCLK, SDATA, and LE control the data transfer. When LE (latch enable) goes high, the 24 bits that have been clocked into the input register on each rising edge of SCLK will be transferred to the appropriate latch. See Figure 1 for the Timing Diagram and Table I for the Latch Truth Table.

The maximum allowable serial clock rate is 20 MHz. This means that the maximum update rate possible for the device is 833 kHz or one update every 1.2 ms. This is certainly more than adequate for systems with typical lock times in hundreds of microseconds.

### ADuC812 Interface

Figure 11 shows the interface between the ADF4001 family and the ADuC812 MicroConverter®. Since the ADuC812 is based on an 8051 core, this interface can be used with any 8051-based microcontroller. The MicroConverter is set up for SPI master mode with CPHA = 0. To initiate the operation, the I/O port driving LE is brought low. Each latch of the ADF4001 family needs a 24-bit word. This is accomplished by writing three 8-bit bytes from the MicroConverter to the device. When the third byte has been written, the LE input should be brought high to complete the transfer.

On first applying power to the ADF4001 family, it needs three writes (one each to the R counter latch, the N counter latch, and the initialization latch) for the output to become active.

I/O port lines on the ADuC812 are also used to control power-down (CE input) and to detect lock (MUXOUT configured as lock detect and polled by the port input).

When operating in the mode described, the maximum SCLOCK rate of the ADuC812 is 4 MHz. This means that the maximum rate at which the output frequency can be changed will be 166 kHz.

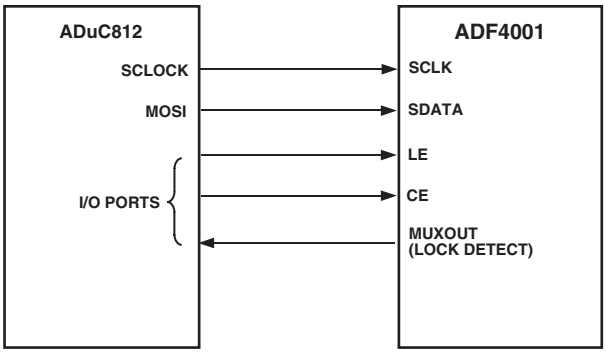


*Figure 11. ADuC812 to ADF4001 Family Interface*

### ADSP-2181 Interface

Figure 12 shows the interface between the ADF4001 family and the ADSP-21xx digital signal processor. The ADF4001 family needs a 24-bit serial word for each latch write. The easiest way to accomplish this using the ADSP-21xx family is to use the autobuffered transmit mode of operation with alternate framing. This provides a means for transmitting an entire block of serial data before an interrupt is generated. Set up the word length for 8 bits and use three memory locations for each 24-bit word. To program each 24-bit latch, store the three 8-bit bytes, enable the autobuffered mode, and then write to the transmit register of the DSP. This last operation initiates the autobuffer transfer.

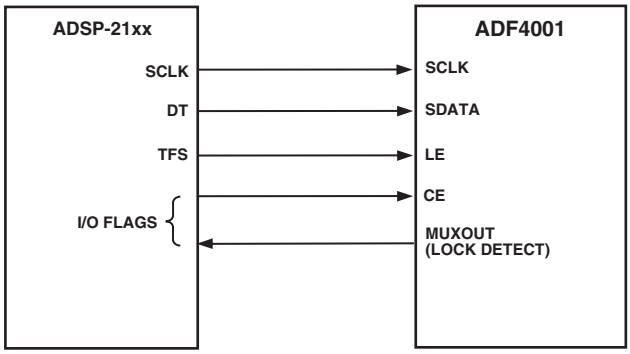


*Figure 12. ADSP-21xx to ADF4001 Family Interface*

## PCB DESIGN GUIDELINES FOR CHIP SCALE PACKAGE

The leads on the chip package (CP-20) are rectangular. The printed circuit board pad for these should be 0.1 mm longer than the package lead length and 0.05 mm wider than the package lead width. The lead should be centered on the pad to ensure that the solder joint size is maximized.

The bottom of the chip scale package has a central thermal pad. The thermal pad on the printed circuit board should be at least as large as this exposed pad. On the printed circuit board, there should be a clearance of at least 0.25 mm between the thermal pad and the inner edge of the pad pattern. This will ensure that shorting is avoided.

Thermal vias may be used on the printed circuit board thermal pad to improve thermal performance of the package. If vias are used, they should be incorporated in the thermal pad at 1.2 mm pitch grid. The via diameter should be between 0.3 mm and 0.33 mm, and the via barrel should be plated with 1 oz. copper to plug the via.

The user should connect the printed circuit board thermal pad to AGND.

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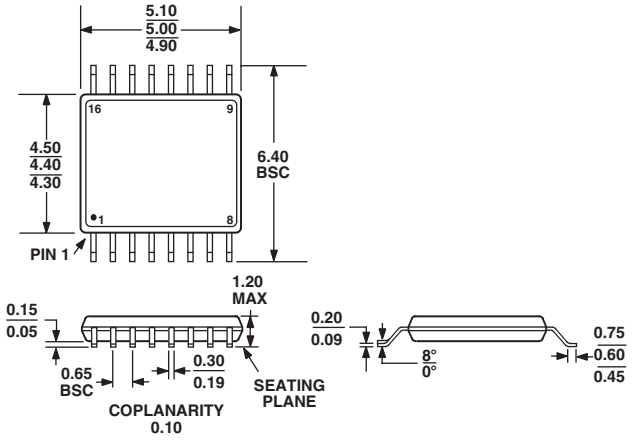
## OUTLINE DIMENSIONS

**16-Lead Thin Shrink Small Outline Package [TSSOP]**
**(RU-16)**
Dimensions shown in millimeters




COMPLIANT TO JEDEC STANDARDS MO-153AB

**20-Lead Lead Frame Chip Scale Package [LFCSP]**
**(CP-20)**
Dimensions shown in millimeters

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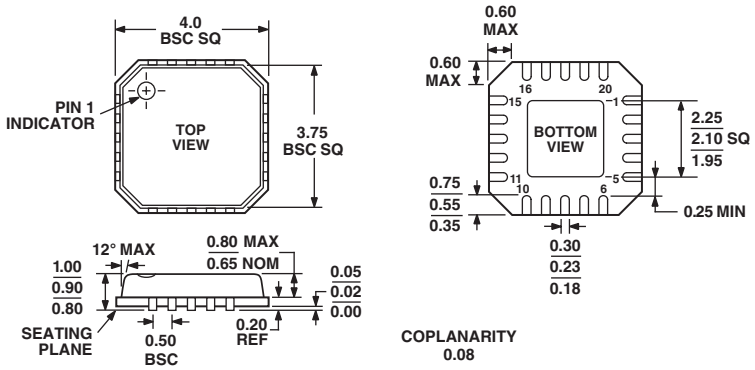


COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-1

# Revision History

| Location | Page |
|---|---|
| **10/03—Data Sheet changed from REV. 0 to REV. A.** | |
| Changes to SPECIFICATIONS | 2 |
| Edits to ORDERING GUIDE | 3 |
| Changes to PIN CONFIGURATIONS | 4 |
| Updated OUTLINE DIMENSIONS | 16 |

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C02569–0–10/03(A)